**ECE 3663 Design Review 1 - Report**

**Group: ADD**

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***Group Progress*:**

For this design review, we built the 16-bit AND, OR, PASS, and 8:1 MUX function blocks for our ALU design. For each of these functions, we first built the sub-circuit for one bit location (e.g. a simple two input AND gate) and then used the saved sub-circuit to build the 16-bit function block. In order to prove that each function works as expected, we simulated each circuit with buffered inputs (double-inverted inputs) and an inverter with transistors four times the minimum size in Cadence as the driven load. The simulation shows that each component works for all combinations of inputs for 1-bit location.

We also drawn a block diagram of the ALU block we are to use in the DSP system design. The ALU can perform 8 different functions: NOP, ADD, SUB, SHIFT, AND, OR, PASS and MULTIPLICATION (for our arbitrary function). It has inputs A, B and Control. Control is the selection input to the 8:1 MUX, the MUX passes the selected function to perform on A and B. Two inputs and ALUout are 16 bits, while Control is 3-bit wise and CarryOut has only 1 bit.

***Ideas for Arbitrary Function:***

Multiplication of the lower 8 bits of inputs A and B.

***Remaining Tasks*:**

We have constructed the basic structure of the ALU block that will be used in the DSP system. Before the next design review, we are to finish the design of the components: ADD, SUB, SHIFT, and our arbitrary function block. We will also feed in inputs and connect outputs for the ALU, and have the three registers working.

After the design review 2, we will work with the project metric – lowest *(Active Power)\*Delay^2\*Area*, and adjust our gates’ sizes and circuitry to reach the best performance and lowest design metric. Then we will pull components together, finalize the DSP design, and work on our project paper and presentation.